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10/598,360	08/25/2006	Hisashi Sugie	40404.33/mo	3155

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EXAMINER	
PHAM, EMILY P	
ART UNIT	**PAPER NUMBER**
2838	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/598,360	SUGIE ET AL.	
	Examiner	Art Unit	
	EMILY PHAM	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 8/25/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "current controlling transistor" must be shown or the feature(s) canceled from the claim(s) 2 and 9. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to because line 5 of page 16 of specification defines "proportional current" as I1/N, however specification does not provide information about N to complete the definition of "proportional current". Can N be any number?

4. The disclosure is objected to because it does not provide sufficient information about "current controlling transistor" disclosed in claims 2 and 9.

Appropriate correction is required.

Claim Objections

5. Claim 9 is objected to because of the following informalities: line 4 of claim 9 has unknown character "=". Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "a proportional current" in line 5. There is insufficient antecedent basis for this limitation in the claim because specification does not provide enough information to define "proportional current" (see Specification above).

Claim 2 recites the limitation "a proportional current" in line 9. There is insufficient antecedent basis for this limitation in the claim because specification does not provide enough information to define "proportional current". Claim 2 recites the limitation "a current controlling transistor" in line 2, this limitation is not supported by drawing and specification. See Drawing and Specification above.

Claim 8 recites the limitation "a proportional current" in line 12. There is insufficient antecedent basis for this limitation in the claim because specification does not provide enough information to define "proportional current" (see Specification above).

Claim 9 recites the limitation "a proportional current" in line 15. There is insufficient antecedent basis for this limitation in the claim because specification does not provide enough information to define "proportional current". Claim 9 recites the limitation "a current controlling transistor" in line 3, this limitation is not supported by drawing and specification. See Drawing and Specification above.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto et al. (USP 6,424,131).

Regarding independent claim 1: Yamamoto et al. **(FIG 1, FIG 5A)** disclose a current detection circuit, characterized by comprising: a first transistor **(1)** for supplying load current to a load **(3)**; a current detection transistor **(2)** having a control electrode receiving the same control signal **(control signal from control circuit 11)** as applied to the control electrode of said first transistor **(1)**, said current detection transistor **(2)** adapted to supply a proportional current that is proportional to said load current; a buffer circuit having an idling current source **(current source 12 provides current to node Q)** for supplying a predetermined idling current to an output node of said current detection transistor **(2)**, said buffer circuit adapted to equalize the output voltage of said first transistor **(1)** with the voltage at said output node of said current detection transistor **(2)**, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current; and a conversion circuit **(6)** for converting into an output signal said detection current outputted from said buffer circuit **(col. 16, line 50 – col. 39, line 62)**.

Regarding independent claim 2: Yamamoto et al. **(FIG 1, FIG 5A)** disclose a current detection circuit, characterized by comprising: a current controlling transistor having a control electrode and an output electrode connected to said control electrode; a variable-current type control-current supplying current source for flowing controlled

current through said current controlling transistor; a first transistor **(1)** connected to said current controlling transistor in a current mirror configuration for supplying load current to a load **(3)**; a current detection transistor **(2)** connected to said current controlling transistor in a current mirror configuration for supplying a proportional current that is proportional to said load current; a buffer circuit having an idling current source **(current source 12 provides current to node Q)** for providing a predetermined idling current to the output node **(Q)** of said current detection transistor **(2)**, said buffer circuit adapted to equalize the output voltage of said first transistor **(1)** with the voltage at said output node of said current detection transistor **(2)**, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current; and a conversion circuit **(6)** for converting into an output signal said detection current outputted from said buffer circuit **(col. 16, line 50 – col. 39, line 62)**.

Regarding dependent claim 3: Yamamoto et al. **(FIG 1, FIG 5A)** disclose the current detection circuit, characterized in that said buffer circuit has: an amplifier **(4)** fed with the output voltage of said first transistor **(1)** and the voltage appearing at the output node of said current detection transistor **(2)**; and a third transistor **(5)** provided between said output node **(Q)** of said current detection transistor **(2)** and said conversion circuit **(6)**, and controlled by the output of said amplifier **(col. 16, line 50 – col. 39, line 62)**.

Regarding dependent claim 4: Yamamoto et al. **(FIG 1, FIG 5A)** disclose the current detection circuit, characterized in that the power supply voltage supplied to said idling current source **(current source 12 provides current to node Q)** is equal to or

higher than the first power supply voltage supplied to said first transistor **(1)** and said current detection transistor **(2)**.

Regarding dependent claim 5: Yamamoto et al. **(FIG 1, FIG 5A)** disclose the current detection circuit, characterized by further comprising: a switching circuit provided in said idling current source **(current source 12 provides current to node Q)**; a comparator for generating a comparison output to switch off said switching circuit when said output signal exceeds a reference level **(col. 16, line 50 – col. 39, line 62)**.

Regarding dependent claim 6: Yamamoto et al. **(FIG 1, FIG 5A)** disclose the current detection circuit, characterized in that said comparator has a characteristic hysteresis having a predetermined hysteresis width **(col. 16, line 50 – col. 39, line 62)**.

Regarding dependent claim 7: Yamamoto et al. **(FIG 1, FIG 5A)** disclose the current detection circuit, characterized by further comprising: a switching circuit provided in said idling current source **(current source 12 provides current to node Q)** and switched on by an idling signal; and a timing circuit for outputting said idling signal for a first predetermined period of time upon receipt of said control command signal and for outputting said control signal after a second predetermine time has elapsed since the receipt of said control command signal, said second predetermine time being shorter than said first predetermined time **(col. 16, line 50 – col. 39, line 62)**.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (USP 6,424,131).

Regarding independent claim 8: Yamamoto et al. **(FIG 8A – FIG 8D)** disclose a load drive circuit for performing pulse-width-modulated (PWM) driving of a single-/multi-phase load **(3)**, said load drive circuit having at least two series circuits such that each of said series circuits includes: a first transistor **(1)** coupled between a first power supply voltage and the output node connected to said load **(3)** to supply load current to said load **(3)** when switched on by a switching signal; and a second transistor coupled between a second power supply voltage and said output node and switched on and off by a PWM switching signal, and that said series circuits together form a single-/multi-phase bridge circuit for driving said single-/multi-phase load **(3)**, said load drive circuit characterized in that: each of said series circuits comprises: a current detection transistor **(2)** receiving the same switching signal as the switching signal supplied to said first transistor **(1)** to provide a proportional current proportional to said load current; and a buffer circuit having an idling current source **(current source 12 provides current to node Q)** for providing a predetermined idling current to the output node of said current detection transistor **(2)**, said buffer circuit adapted to equalize the output voltage of said first transistor **(1)** with the voltage at said output node of said current detection transistor **(2)**, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current, and characterized in that said

load drive circuit further comprises a conversion circuit **(6)** for collectively converting into an output signal the detection currents outputted from the respective buffer circuits **(col. 16, line 50 – col. 39, line 62)**. **Yamamoto et al. do not disclose separate power supply voltages for each series connected circuits, however it would have been an obvious matter of design choice to have 2 power supply voltages of different values for two series circuits for the purpose of providing 2 different uninterrupted idling currents. Claim 8 only discloses duplication of circuit recited in claim 1 to operate the multi-phase bridge circuit formed of more than one series circuit; it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ8.**

Regarding independent claim 9: Yamamoto et al. **(FIG 8A – FIG 8D)** disclose a load drive circuit having at least two current output circuits to form a single-/multi-phase bridge circuit for driving a single-/multi-phase load **(3)**, each of said current output circuits including: a current controlling transistor having a control electrode and an output electrode connected to said control electrode;=control-current supplying current source for supplying controlled current to said current controlling transistor; a first transistor **(1)** connected to said current controlling transistor in a current mirror configuration and provided between a first power supply voltage and the output node of said load drive circuit supplying load current to said load **(3)**; and a second transistor connected between said output node and a second power supply voltage and configured to be switched on and off by a switching signal, said load drive circuit

characterized in that each of said current outputting circuit comprises, in association with the first transistor **(1)** thereof: a current detection transistor **(2)**, connected to said current controlling transistor in a current mirror configuration for supplying a proportional current that is proportional to said load current; and a buffer circuit having an idling current source **(current source 12 provides current to node Q)** for providing a predetermined idling current to the output node of said current detection transistor **(2)**, said buffer circuit adapted to equalize the output voltage of said first transistor **(1)** with the voltage at said output node of said current detection transistor **(2)**, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current, and characterized in that said load drive circuit comprises a conversion circuit **(6)** for collectively converting the detection currents outputted from the respective buffer circuits into an output signal **(col. 16, line 50 – col. 39, line 62)**. **Yamamoto et al. do not disclose separate power supply voltages for each series connected circuits, however it would have been an obvious matter of design choice to have 2 power supply voltages of different values for two series circuits for the purpose of providing 2 different uninterrupted idling currents. Claim 9 only discloses duplication of circuit recited in claim 1 to operate the multi-phase bridge circuit formed of more than one series circuit; it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ8.**

Regarding dependent claim 10: Yamamoto et al. **(FIG 8A – FIG 8D)** disclose the load drive circuit, characterized in that said buffer circuit has: an amplifier fed with the

output voltage of said first transistor **(1)** and the voltage appearing at the output node of said current detection transistor **(2)**; and a third transistor provided between said output node of said current detection transistor **(2)** and said conversion circuit **(6)**, and controlled by the output of said amplifier.

Regarding dependent claim 11: Yamamoto et al. **(FIG 8A – FIG 8D)** disclose the load drive circuit, characterized by further comprising: a switching circuit provided in said idling current source **(current source 12 provides current to node Q)**; and a comparator for generating a comparison output when said output signal exceeds said reference level, to thereby switch off said switching circuit by said comparison output **(col. 16, line 50 – col. 39, line 62)**.

Regarding dependent claim 12: Yamamoto et al. **(FIG 8A – FIG 8D)** disclose the load drive circuit, characterized by further comprising: a switching circuit provided in said idling current source **(current source 12 provides current to node Q)** and switched on by an idling signal; and a timing circuit for outputting said idling signal for a first predetermined period of time upon receipt of said control command signal and for outputting said control signal after a second predetermine time has elapsed since the receipt of said control command signal, said second predetermine time being shorter than said first predetermined time **(col. 16, line 50 – col. 39, line 62)**.

Regarding dependent claim 13: Yamamoto et al. **(FIG 8A – FIG 8D)** disclose a memory storage characterized by comprising: a load drive circuit; and a motor driven by said load drive circuit **(col. 16, line 50 – col. 39, line 62)**.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Jackson (USP 6,424,131) discloses bias regulator with sense-switched load.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EMILY PHAM whose telephone number is (571)270-3046. The examiner can normally be reached on Mon-Thu (7:00AM - 6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on (571) 272 - 2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 2, 2008

/Jessica Han/
Primary Examiner, Art Unit 2838

EP